

Abstract of the Disclosure

In the semiconductor device of the present invention, a plurality of dummy patterns are formed in a grid arrangement in the scribe line areas of a wafer, and a plurality of dummy patterns are formed in a diagonally forward skipped arrangement in the chip interior areas of the wafer. Altering the arrangement of dummy patterns in the chip interior areas and scribe line areas in this way enables formation of dummy patterns with greater uniformity in the chip interior areas and enables formation of dummy patterns with greater resistance to loss that occurs when dicing in scribe line areas.